OIPE
APR 21 2004
PATENT & TRADEMARK OFFICE

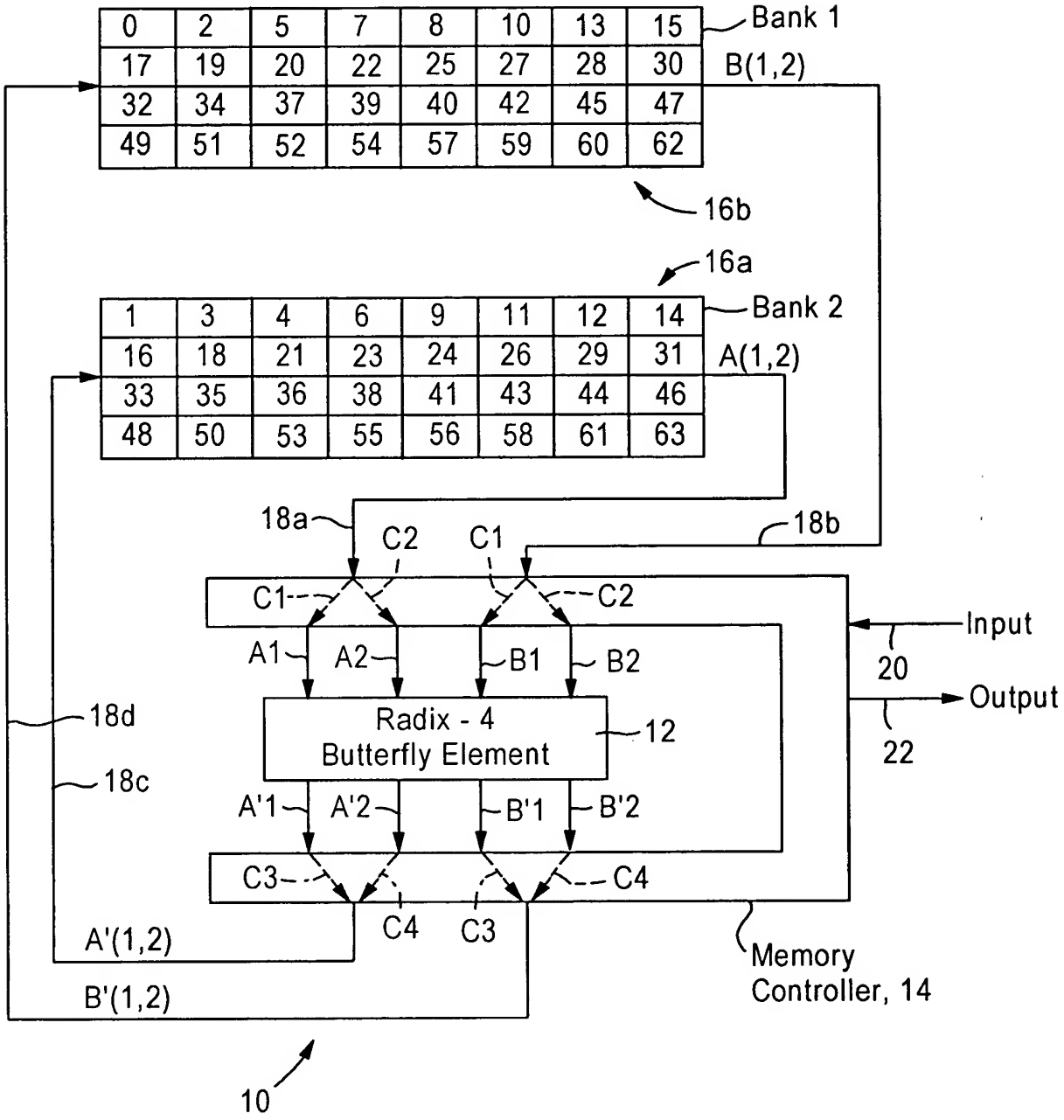

Figure 1

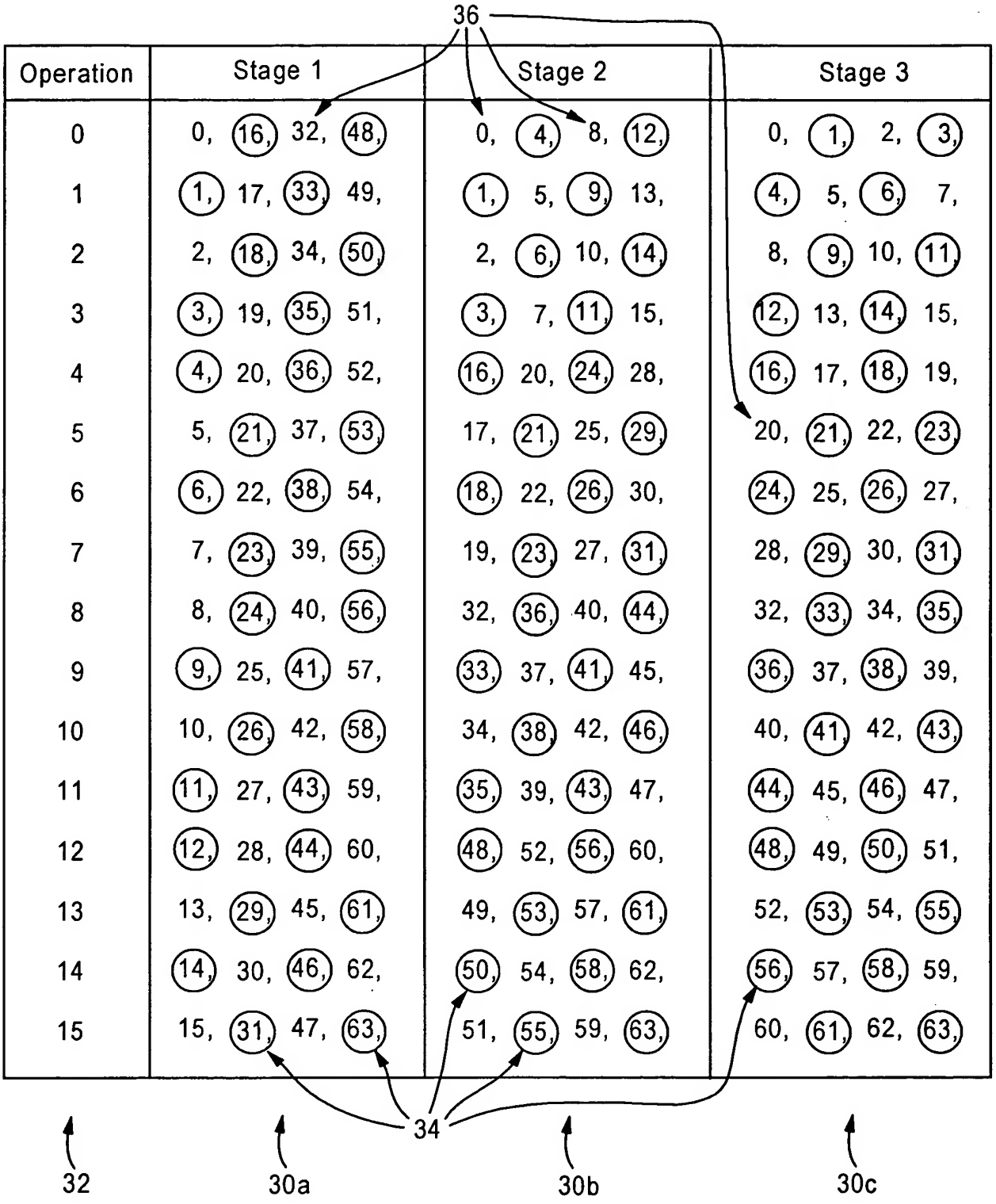
36
Operation
Stage 1
Stage 2
Stage 3
0 0, 16, 32, 48, 0, 4, 8, 12, 0, 1, 2, 3,
1 1, 17, 33, 49, 1, 5, 9, 13, 4, 5, 6, 7,
2 2, 18, 34, 50, 2, 6, 10, 14, 8, 9, 10, 11,
3 3, 19, 35, 51, 3, 7, 11, 15, 12, 13, 14, 15,
4 4, 20, 36, 52, 16, 20, 24, 28, 16, 17, 18, 19,
5 5, 21, 37, 53, 17, 21, 25, 29, 20, 21, 22, 23,
6 6, 22, 38, 54, 18, 22, 26, 30, 24, 25, 26, 27,
7 7, 23, 39, 55, 19, 23, 27, 31, 28, 29, 30, 31,
8 8, 24, 40, 56, 32, 36, 40, 44, 32, 33, 34, 35,
9 9, 25, 41, 57, 33, 37, 41, 45, 36, 37, 38, 39,
10 10, 26, 42, 58, 34, 38, 42, 46, 40, 41, 42, 43,
11 11, 27, 43, 59, 35, 39, 43, 47, 44, 45, 46, 47,
12 12, 28, 44, 60, 48, 52, 56, 60, 48, 49, 50, 51,
13 13, 29, 45, 61, 49, 53, 57, 61, 52, 53, 54, 55,
14 14, 30, 46, 62, 50, 54, 58, 62, 56, 57, 58, 59,
15 15, 31, 47, 63, 51, 55, 59, 63, 60, 61, 62, 63,
34
32
30a
30b
30c

Figure 2

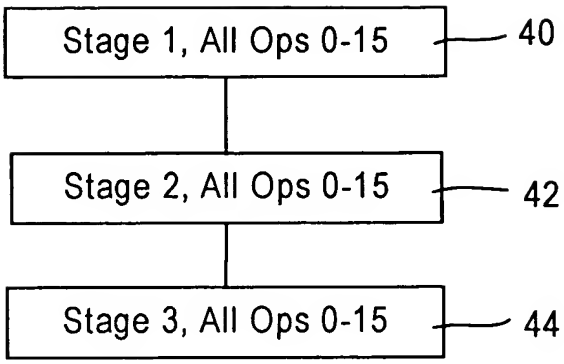

Figure 3A

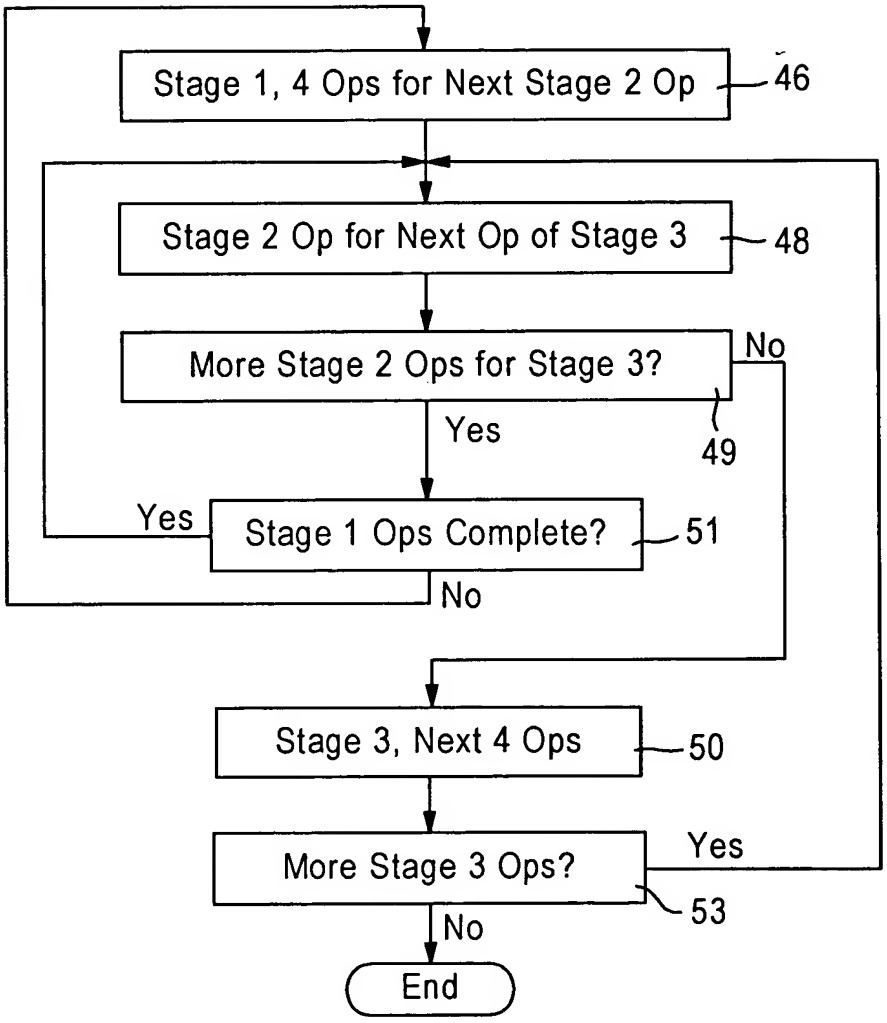

Figure 3B

Bank 1 Read	0	32	17	49	2	34	19	51	20	52	5	...	47	0	8	5	13	2	10	7	...	0	2	5	7	8	10	13
Bank 2 Read	16	48	1	33	18	50	3	35	4	36	21	...	63	4	12	1	9	6	14	3	...	1	3	4	6	9	11	12
Bank 1 Write			0	32	17	49	2	34	19	51	20	...	62	15	47	0	8	5	13	2	...	51	59	0	2	5	7	8
Bank 2 Write			16	48	1	33	18	50	3	35	4	...	46	31	63	4	12	1	9	6	...	55	63	1	3	4	6	9
Stage 1 Op	(0)	(0)	0	(1)	1	(2)	2	(3)	3	(4)	4	...	(15)	15	D	D	D	D	D	D		D	D	D	D	D	D	D
Stage 2 Op														(0)	(0)	0	(1)	1	(2)	2	...	15	D	D	D	D	D	D
Stage 3 Op																						(0)	(0)	0	(1)	1	(2)	2
Clock Cycle	1	2	3	4	5	6	7	8	9	10	11	...	32	33	34	35	36	37	38	39	...	65	66	67	68	69	70	71

66 68

60 62 64

Figure 4A

Bank 1 Read	0	32	20	52	8	40	28	60	0	8	17	49	5	27	25	57	13	45	5	9	2	...	0	2	5	7	8	11
Bank 2 Read	16	48	4	36	24	56	12	44	4	12	1	33	21	53	9	41	29	61	1	13	18	...	1	3	4	6	9	10
Bank 1 Write			0	32	20	52	8	40	28	60	0	8	17	49	5	27	25	57	13	45	5	...	7	15	0	2	5	7
Bank 2 Write			16	48	4	36	24	56	12	44	4	12	1	33	21	53	9	41	29	61	1	...	3	11	1	3	4	6
Stage 1 Op	(0)	(0)	0	(4)	4	(8)	8	(12)	12		(1)	(1)	1	(5)	5	(9)	9	(13)	13	(2)	(2)	...						
Stage 2 Op									(0)	(0)	0								(1)	(1)	1	...	3					
Stage 3 Op																						...	(0)	(0)	0	(1)	1	(2)
Clock Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	...	41	42	43	44	45	46

78 80

60 62 70 72 74 76

Figure 4B

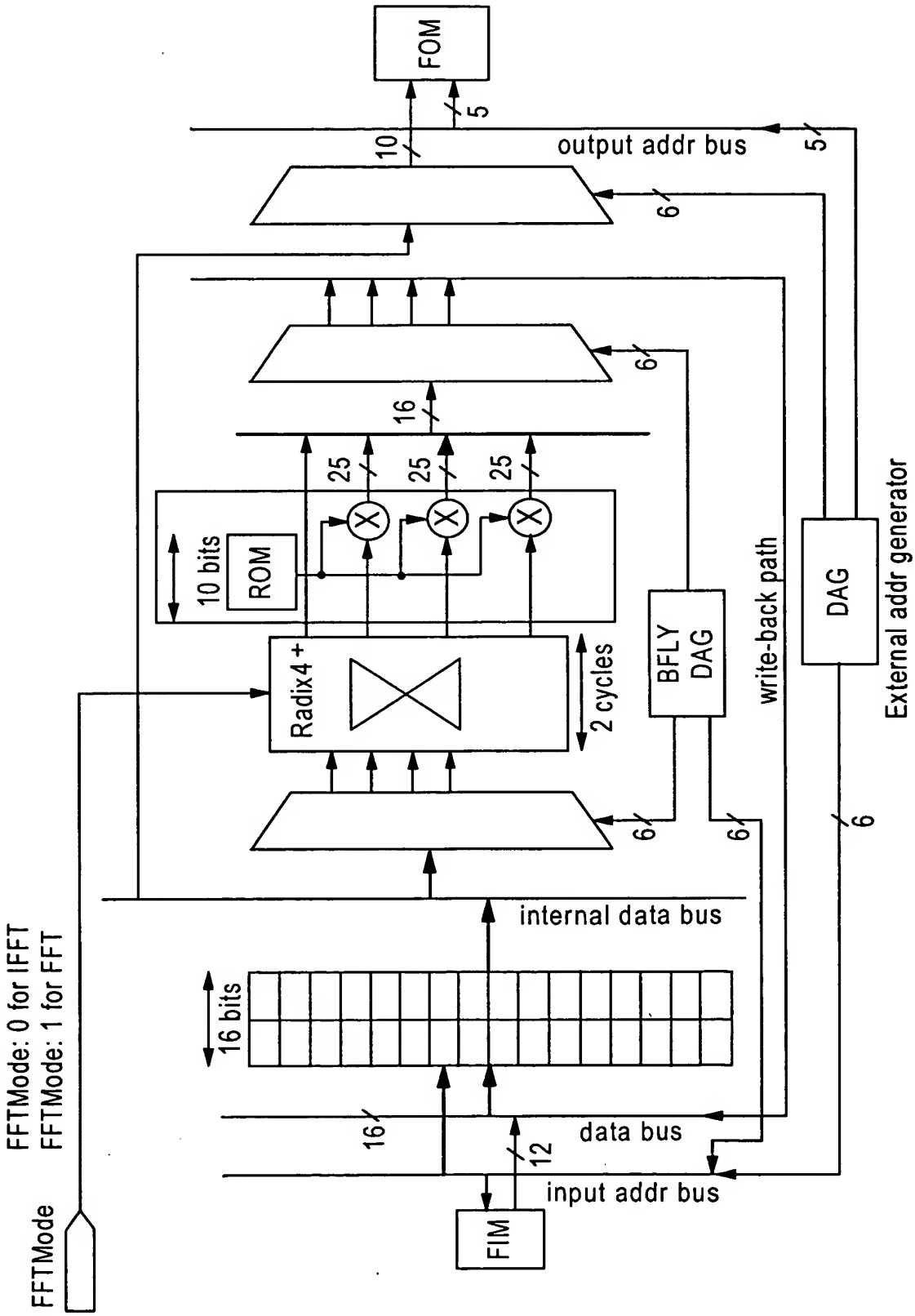
FOM
5
10
output addr bus
5
6
6
16
25
25
25
10 bits
ROM
Radix4 +
2 cycles
BFLY DAG
write-back path
DAG
External addr generator
6
6
6
internal data bus
16 bits
16
data bus
12
input addr bus
FIM
FFTMode
FFTMode: 0 for IFFT
FFTMode: 1 for FFT

Figure 5